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15 Feb 2016

Airworthiness Directive

16/2016

Complex Electronic Hardware Development and Certification

CENTRE FOR MILITARY AIRWORTHINESS & CERTIFICATION (CEMILAC)

DEFENCE RESEARCH & DEVELOPMENT ORGANIZATION

MINISTRY OF DEFENCE, GOVT OF INDIA

Documentation Page

Document Classification:	**Unclassified**		
Doc. No:	**16/2016**		
Doc. Date:	15 Feb 2016	**No. of Pages:**	17
Doc. Title:	Airworthiness Directive on Complex Electronic Hardware Development and Certification		
Key Words:	Complex Electronic Hardware (CEH), Design Entry, Simulation, Certification, Stage of Involvement (SoI), Level of CEMILAC Involvement		
Project No:	NA		
Abstract:	Akin to qualification of hardware, the constituent software and custom micro coded components called as Complex Electronic Hardware (CEH) of a system or subsystem needs qualification. Hardware and Software qualification has been well established in the Defence Avionics Industry. Of late, qualification of CEH is gaining importance due to the complexity and volume of algorithms/logic being built into it. CEH includes FPGAs, ASICs, PLDs etc. This directive will focus on the development and certification aspects of CEH.		
Organisation Address: CEMILAC, DRDO, Min. of Defence, Marathahalli Colony PO, Bangalore 37			
Distribution List: Concerned DRDO Labs, PSUs, DGAQA and Users			
Prepared By:	**Systems Group, CEMILAC**		
Feedback From:	**Concerned DRDO Labs, PSUs, DGAQA and Users**		
Approved By:	**P Jayapal** **Chief Executive (Airworthiness)** **CEMILAC, DRDO**		
Revision No:	**Issue – 1.0**		

Revision History

Document Title	:	Complex Electronic Hardware Development and Certification	
Document Number	:	16 / 2016	
Revision Number	**Date**	**Approval**	**Remarks**
Issue - 0.1	14 Dec 2015	----	Draft for Review
Issue - 0.2	08 Jan 2016	----	Comments incorporated
Issue - 1.0	15 Feb 2016	CE(A)	Final

Contents

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1 Introduction

1.1 Purpose

Airborne Electronics systems are presently designed widely with Complex Electronic Hardware (CEH) like Field Programmable Gate Arrays (FPGAs), Application Specific Integrated Circuits (ASICs) and other Programmable Logic Devices (PLDs). In Indian military avionics also, the trend of using CEH has increased. Even currently, many of the processor based applications are getting replaced with CEH. Almost all the electronics is bound to have CEH because of its flexible / reliable programming that can be obtained when compared to processor based software.

The use of CEH for safety and mission critical aircraft applications are posing new safety and certification challenges. These challenges arise from the concern that, implementation of aircraft functions in CEH is vulnerable to the adverse effects of hardware design errors. To alleviate this risk, it has become necessary to ensure that hardware design is addressed in a more consistent and verifiable manner during both the design and certification processes.

Hence, it becomes necessary to formulate a directive for Development and Certification of CEH in the Indian military airborne applications.

1.2 Scope

The Scope of this directive is to address the major activities and artefacts involved in Design, Development and Certification of **C**omplex **E**lectronic **H**ardware (**CEH**) for Indian Military airborne applications.

1.3 Applicability

This directive is applicable from the date of release.

1.4 References

a. Procedure for Design, Development and Production of Military Aircraft and Airborne Stores DDPMAS 2002 and DDPMAS-2002, Vol-II, Software Development and Certification.
b. DO-254, *Design Assurance Guidance for Airborne Electronic Hardware*, published by RTCA, Inc., *2000*
c. FAA Order 8110.105 CHG 1,*Simple And Complex Electronic Hardware Approval Guidance, 2008*
d. SAE/ARP 4761, (Aerospace Recommended Practice 4761A) Guidelines and methods for conducting the safety assessment process on civil airborne systems and equipment, 1996-12

1.5 Acronyms

i.	CDD	Conceptual Design Data
ii.	DDD	Detail Design Data
iii.	HAS	Hardware Accomplishment Summary
iv.	HATC	Hardware Acceptance Test Criteria
v.	HCI	Hardware Configuration Index
vi.	HCMP	Hardware Configuration Management Plan
vii.	HCMR	Hardware Configuration Management Records
viii.	HCS	Hardware Coding Standard

ix.	HDL	Hardware Description Language
x.	HDP	Hardware Development Plan
xi.	HDS	Hardware Design Standard
xii.	HECI	Hardware Environment Configuration Index
xiii.	HPAP	Hardware Process Assurance Plan
xiv.	HPAR	Hardware Process Assurance Records
xv.	HRAP	Hardware Reviews and Analysis Procedures
xvi.	HRAR	Hardware Reviews and Analysis Results
xvii.	HRD	Hardware Requirements Data
xviii.	HRS	Hardware Requirement Standard
xix.	HTD	Hardware Traceability Data
xx.	HTP	Hardware Test Plan
xxi.	HTR	Hardware Test Results
xxii.	HVVP	Hardware Verification and Validation Plan
xxiii.	HVVS	Hardware Verification and Validation Standards
xxiv.	IRD	Interface Requirements Data
xxv.	PHAC	Plan for Hardware Aspects of Certification
xxvi.	PR	Problem Reports
xxvii.	RTL	Register Transfer Level
xxviii.	SSA	System Safety Assessment
xxix.	TAQD	Tool Assessment and Qualification Data

2 CEH Life Cycle

2.1 Simple Electronic Hardware (SEH)

A hardware item is considered simple if a comprehensive combination of deterministic tests and analyses appropriate to the Design Assurance Level (DAL) can ensure correct and complete functional performance under all foreseeable operating conditions, with no anomalous behaviour.

2.2 Complex Electronic Hardware (CEH)

A hardware item that is not simple is considered to be 'complex'. System design team shall classify a given hardware item into SEH/CEH early in project.

2.3 Hardware Item

For this directive, a hardware item is defined as any custom micro coded component that is programmed by the developer. Hardware item includes, but not limited to FPGAs, ASICs, PLDs, PALs. It also covers those similar electronic components used in the design of aircraft systems and equipment.

2.4 Safety Assessment (SA)

System Engineering Process shall identify and allocate system requirements to be implemented through CEH. Safety Assessment Process shall be followed to determine the Design Assurance Level for CEH. ARP 4761 or MIL-STD-882 can be used for Safety Assessment (SA) Process.

2.5 Independent Verification & Validation (IV&V)

IV&V is a team of people from system experts, designer's IV&V team, CEMILAC, DGAQA and user representative. The constitution of the IV&V team for review of the artefacts at different phases will be addressed in PHAC and HVVP documents.

2.6 CEH Life Cycle Activities

CEH lifecycle activities are shown in Fig 1. CEH Life cycle begins with the allocation of System requirements to CEH. There is a continuous flow of information from CEH life cycle to System Engineering process like fault containment boundaries/ failure recovery, CEH verification activities to be performed at system level etc. The CEH life cycle includes Planning Process, Hardware Design Process and Supporting Processes. Planning process involves planning for hardware aspects of certification and related other plans. Hardware Design Process includes activities like Requirements capture, Conceptual and Detailed Design, and Implementation. Conceptual Design and Detailed Design may be merged into one for less complicated programs and appropriately documented in the Plans. The CEH will be programmed as per approved hardware configuration, during production process. Supporting Processes provide umbrella activities covering the whole CEH life cycle span. Model based Design and development is not addressed in the life cycle process described in this document.

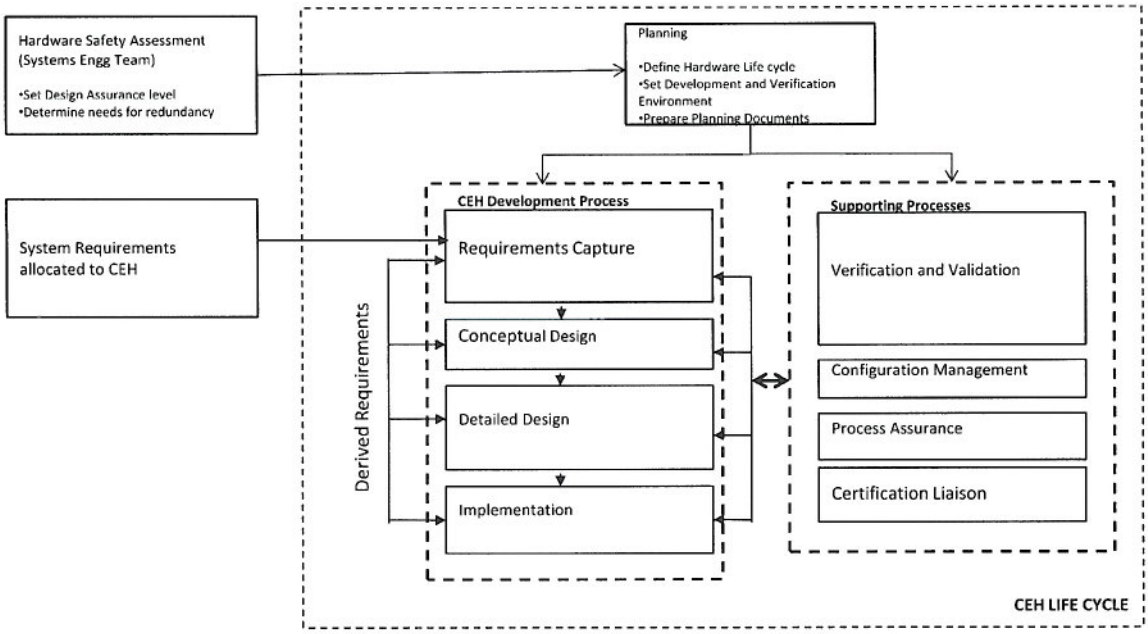

Fig 1. CEH: Life Cycle Activities

2.6.1 Planning Phase

Planning phase describes the CEH planning process which is used to control the development of the CEH item. This process produces the hardware plans, which may be contained in one or more documents. Standard documents covering specific hardware design life cycle processes, such as configuration management or process assurance, are acceptable provided they meet the planning objectives for the applicable process.

The planning process establishes the various hardware plans, standards, procedures, activities, methods, and tools required to develop, verify and maintain the hardware life cycle data.

Documents and Process for Planning Phase:

Supplier of Inputs	**Inputs**	**Process**	**Output of the Process**	**Users of the outputs**
System Engineer	-Technical/ Functional Specification of the LRU allocated to CEH -SSA document	Preparation of planning documents	PHAC HCMP HVVP, HPAP HDP HRS, HDS, HVVS, HCS Tool Qual Assessment data (if applicable)	CEMILAC, QA, IV&V, DGAQA
HW Designer /CEH Designer		Identifying the criticality level allocated to CEH		

Verification of the Planning Phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Stage of Involvement
HW/ RTL Designer	All previous outputs in this phase	Review by IV&V, Audit by QA	Inputs Base-lined HRAR, HPAR	SoI-1

Note: In this phase, Hardware Traceability Data (HTD) to be made w.r.t. all the outputs and inputs.

2.6.2 Development Phase

2.6.2.1 Requirements Capture

The Requirement process establishes the requirements of CEH to produce the hardware life cycle data. Requirements are identified, defined and documented. The requirements specify the functional, performance, safety, quality, maintainability, and reliability requirements for the hardware item being developed. During this phase, the activities of the designer and verification engineer are given below along with the necessary outputs. Review activity of the same phase is also given.

Documents and Process for Requirement Phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Users of the outputs
HW/CEH Designer	All Plans and HRS -Technical/ Functional Specification of the LRU allocated to CEH -SSA document	Developing detailed functional requirements allocated to CEH by the HW/CEH designer Developing Redundancy Requirements based on SSA	HRD IRD	CEMILAC, QA, IV&V, DGAQA
Verification Engineer		Developing behavioural specifications for testing of CEH	HTP (HL), HRAP	

Verification of the Requirement phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Stage of Involvement
Designer/Verification Engr	All previous outputs in this phase	Review by IV&V, Audit by QA	Baselined HRD, IRD, HTP (HL), HRAP, HRAR, HPAR	SoI-2

Note: In this phase, Hardware Traceability Data (HTD) to be made w.r.t. all the outputs and inputs.

2.6.2.2 Conceptual Design

Architectural design of the CEH to be brought out in Conceptual design phase. During this phase, the activities of the designer and verification engineer are given below along with the necessary documents. Review activity of the same phase is also given.

Documents and Process for Conceptual Design Phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Users of the outputs
CEH Designer	HRD IRD , HDS	High Level Architecture/ Block representation at component (CEH) level	High Level Arch/Block diagram at CEH level (CDD)	Designer, CEMILAC, QA IV&V DGAQA
Verification Engr	CDD, HVVS	Deriving Test Bench Architecture diagram for CEH	Test Bench Arch Diag	

Verification of the Conceptual Design phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Stage of Involvement
Designer/Verification Engr	All the previous outputs in this phase	Review by IV&V	Baselined CDD, Test bench Arch Blk Diag, HRAR	SoI-2

Note: In this phase, Hardware Traceability Data (HTD) to be made w.r.t. all the outputs and inputs.

2.6.2.3 Detailed Design:

The Design process establishes the design of CEH to produce the hardware life cycle data. The detailed design process produces detailed design data using the hardware item requirements as the basis for the detailed design. During this phase, the activities of the designer and verification engineer are given below along with the necessary documents. Review activity of the same phase is also given.

Documents and Process for Detailed Design Phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Consumer of the outputs
CEH Designer	CDD, HDS	Converting CEH requirements (HRD/IRD) & CDD into lower level modules	Module level Schematics & Block diagrams, DDD	Designer, CEMILAC, QA IV&V DGAQA
Verification Engineer	Test Bench Arch Block Diagram, DDD, HVVS	Deriving Test procedures for CEH (Test benches)	HTP (LL)	

Verification of the Detailed Design phase:

Supplier of Inputs	Inputs	Process	Output of the Process	Stage of Involvement
Designer	All previous outputs in this phase	Review by a committee, IV&V, Audit by QA	Baselined DDD, HTP (LL), HRAR, HPAR	SoI-2

Note: In this phase, Hardware Traceability Data (HTD) to be made w.r.t. all the outputs and inputs.

2.6.2.4 *Implementation Phase*

The implementation process converts the design of CEH to produce the bit stream (Net list) to be incorporated into the CEH. During this phase, the activities of the designer and IV&V are given below along with the necessary documents. Review activity of the same phase is also given.

Documents and Process for Implementation Phase:

Supplier of Inputs	**Inputs**	**Process**	**Output of the Process**	**Users of the outputs**
CEH Designer	HRD, CDD, DDD, HCS	Develop RTL/HDL code, Synthesis, P&R, define and apply constraints	HDL/RTL code, Netlist, Synthesis Reports	Designer, CEMILAC, QA IV&V DGAQA

Verification of the implementation phase: (IV&V team)

Supplier of Inputs	**Inputs**	**Process**	**Output of the Process**	**Stage of Involvement**
Designer	All previous outputs in this phase	Verification of Net list, code review etc. Implementation of all the requirements to be verified.	HRAR, HPAR	SoI-3

Note: In this phase, Hardware Traceability Data (HTD) to be made w.r.t. all the outputs and inputs.

2.6.2.5 *Testing Phase*

The testing process involves the following activities and documents during testing and its verification stage. Following the CEH testing activity, integration of hardware, software and CEH be taken up during integration testing for combined and integrated checks.

Documents and Process for Testing Phase:

Verification Engineer	HTP (HL/LL) HCS	Developing models and writing test benches /test cases, Perform top level and module level verification by: Behavioural/functional and timing simulation, Coverage Testing, FPGA Timing analysis, In Time/On Target Testing, Integration testing at Board/LRU level etc.	HRAR, HTR, Functional /Gate level simulation reports, Code Coverage reports etc.	Designer, CEMILAC, QA IV&V DGAQA

Verification of the Testing phase: (IV&V team)

Supplier of Inputs	Inputs	Process	Output of the Process	Stage of Involvement
Verification Engineer & Designer	All previous outputs in this phase	Implementation of all the requirements to be verified.	HRAR, HTR (HL/LL), HPAR	SoI-3

Note: In this phase, Hardware Traceability Data (HTD) to be made w.r.t. all the outputs and inputs.

2.6.3 Supporting Processes

2.6.3.1 Verification and Validation: Verification and Validation shall be done as per HVVP. The role of a verification engineer during each phase of CEH life cycle has been discussed above.

2.6.3.2 Configuration Management: The configuration management process is intended to provide the ability to consistently replicate the configuration item, regenerate the information if necessary and modify the configuration item in a controlled fashion if modification is necessary. Configuration Management shall be done as per HCMP.

2.6.3.3 Process Assurance: Process assurance ensures that the life cycle process objectives are met and activities have been completed as outlined in plans or that deviations have been addressed. There is no intent to impose specific organizational structures.

Process assurance activities shall be achieved with independence in order to objectively assess the life cycle process, identify deviations and ensure corrective action. Process assurance shall be done as per HPAP.

2.6.3.4 ***Certification Liaison:*** Certification liaison defines the communication between the system developer and the certification authority, covering how data is approved, joint reviews, and when and how the certifying authority witnesses compliance testing. Certification liaison shall be as per PHAC.

Documents for Certification Completion:

Supplier of Inputs	Inputs	Process	Output of the Process	Stage of Involvement
Applicant	All the baseline documents HCI, HECI, HCMR, HPAR, HAS	Final review of the accomplishments and verification activities of the development lifecycle.	Approved HCI, HECI,HAS	SoI-4

3 Certification Aspects for CEH

3.1 CEH Certification

Certification follows concurrent approach where certification agency will be involved in the complete life cycle of CEH. Each System/LRU shall have a Route to Certification (RTC) document from which PHAC shall be derived during Planning Phase. Stage of Involvement (SOI) and Level of Involvement (LOFI) of Certification agency are documented during the planning process. On satisfactory completion of development and other activities as planned, the CEH item will be certified for use in the airborne electronic hardware.

3.2 Stages of Involvement (SOI)

Life Cycle Phases	Certification Activities
Planning	• Hardware Planning Review (SoI-1)
Requirements	• Hardware Development Review (SoI – 2)
Conceptual Design	
Detailed Design	
Implementation & Testing	• Hardware Verification and Validation Review (SoI-3)
Certification	• HCI, HECI and HAS approval(SoI-4)

1. SoI-1 Hardware Planning Review (End of Planning Process)
2. SoI-2 Hardware Development Review (Midpoint of hardware Design Phase)
3. SoI-3 Hardware Development Review (Midpoint of Implementation Phase)
4. SoI-4 Final Hardware Build

3.3 Level of CEMILAC Involvement

Stage	Process output (Data Items)	CEMILAC level of involvement			
		Level A	Level B	Level C	Level D
Hardware Planning Stage	*Hardware Plans*				
	Plan For Hardware Aspects Of Certification (PHAC)	A	A	A	A
	Hardware Design Plan (HDP)	R	R	R	r
	Hardware Verification & Validation Plan (HVVP)	A	A	R	r
	Hardware Configuration Management Plan (HCMP)	A	A	R	A
	Hardware Process Assurance Plan (HPAP)	A	R	R	A
	Hardware Design Standards (HDS)	R	R	R	r
	Hardware Requirement Standards (HRS)	R	R	R	r
	Hardware Coding Standard (HCS)	R	R	R	r
	Hardware Verification and Validation Standard (HVVS)	R	R	R	r
Hardware Development Stage	*Hardware Design data*				
	Hardware Requirements (HRD)	R	R	R	R
	Hardware Design Representation data(HDRD)				
	Conceptual design Data (CDD)	R	R	R	r
	Detailed Design Data (DDD)	R	R	R	r
	Hardware/Software Interface Data (IRD)	r	r	r	r
Hardware Verification Stage	*Verification & Validation data*				
	Hardware Traceability Data(HTD)	R	R	R	R
	Hardware Review and analysis procedures(HRAP)	R	R	R	r
	Hardware review and Analysis results(HRAR)	R	R	R	r
	Hardware Test Procedures (HTP)	R	R	R	r
	Hardware Test results (HTR)	R	R	R	r
	Tool Assessment and Qualification Data (TAQD)	R	R	-	-
Certification / Final Stage	*Certification*				
	Hardware configuration Management Records (HCMR)	R	R	R	r
	Hardware Accomplishment Summary(HAS)*	R	R	R	R
	Hardware Environmental Configuration Index (HECI)	R	R	R	r
	Hardware Process Assurance records(HPAR)	R	R	R	r
	Hardware Configuration Index (HCI)	A	A	A	A

Level of CEMILAC Involvement: A: Approved, **R**: Reviewed, **r**: Referred

As per DO-254 Levels: A- Catastrophic; B- Hazardous; C- Major; D- Minor; E - No effect

(* Based on Approval of HAS by IV&V, CEMILAC will approve HCI)

4 Additional considerations

4.1 COTS and IP Cores

Software that runs on processors inside CEH will follow DO-178B guidelines for certification. It shall be treated in par with any other software development and certification process. Commercial Off The Shelf (COTS) Intellectual Property (IP) cores are available to speed up CEH development. Certified versions of such COTS IP cores shall be used in safety critical airborne embedded systems. For mission critical and non-critical systems, however, IPs may be used after stipulated validation and assessment process in concurrence with certification/inspection agencies.

Along with the CEH under test, the necessary COTS and IP cores testing/analysis shall be carried out by way of:

i. Extensive COTS IP testing and analysis be carried out so that the system developer gains enough information about the functionality, and how will it operate during boundary conditions. This should include testing and analysis of any functionality from the COTS IP that will not be used or activated in the specific application.
ii. Re-engineering the required life cycle data from known information about the COTS IP functionality and design.
iii. Architectural mitigation at the device, board, LRU or system level that will detect and/or mitigate unforeseen or undesirable CEH operation in which the COTS IP is installed.

4.2 Change in CEH

Whenever there is a change in CEH design/implementation, Problem Reports (PRs) need to be generated. Certain hardware qualification testing which may be affected by the change has to be discussed with certification and inspection agencies and finalized.

4.3 Tool Qualification

Tool Qualification is to be carried out only for safety critical systems. Criticality level of the system is derived out of SA Process. Tool Qualification may be done in line with DO-330 guidelines. Tool Qualification has to be planned as a part of PHAC. Tool Assessment and Qualification Data (TAQD) to be made available before Testing phase.

5 Promulgation

5.1 Promulgation

a. The draft of this directive was circulated to concerned DRDO laboratories, PSUs, DGAQA & Users and feedback obtained. This directive is released after incorporating relevant comments received from various members.

b. Further, during the course of implementing this directive, observations/ improvements if any, may be documented and communicated to CEMILAC immediately, as per the feedback form in Appendix 'A'. This will help in future update of the directive.

c. After two years of release of this directive, feedback received from the stakeholders will be suitably incorporated and a revised version will be released for regular practice.

5.2 Feedback

The feedback, if any, of this directive may please be forwarded as per the format in Appendix 'A' to:

The Chief Executive (Airworthiness)
CEMILAC, Defence Research & Development Organization
Marathahalli Colony Post
Bangalore - 560 037

FEEDBACK FORM (DESIRABLE)

RECOMMEND A CHANGE:	**1. DOC TITLE:** AW Directive on CEH Development and Certification **2. DOC No.:** 16/2016 (Issue 1.0) **3. DOC DATE:** 15 Feb 2016

4. a. NATURE OF CHANGE *(Identify paragraph number and include suggestions / improvements. Attach extra sheets as needed).*

4. b. PROPOSED REWRITE

4. c. 'Nil' COMMENTS | Nil | | **(Put a 'Tick' in the box if 4. a. & 4. b. are empty)**

5. SUBMITTER DETAILS

a. NAME *(Last, First, Middle)*

b. ORGANIZATION

c. ADDRESS *(Include pin code)*

d. TELEPHONE

(i) Landline (Off)

(ii) Mobile

e. DATE SUBMITTED (DDMMYYYY)

6. RECEIVER DETAILS

a. NAME : THE CHIEF EXECUTIVE(AIRWORTHINESS), CEMILAC

b. ADDRESS: THE CHIEF EXECUTIVE(AIRWORTHINESS), CEMILAC, DRDO,

MARATHAHALLI COLONY POST, BANGALORE - 560 037

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28. GM, RWRDC, C/o. HAL Helicopter Division, Bengaluru
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31. GM, SLRDC, HAL, Hyderabad
32. Director Planning, HAL Corporate office, Bengaluru
33. Chairman, HAL Corporate Office, Bengaluru
34. HAL (QA&CS), HAL Corporate Office, Bengaluru
35. CMD, BEL, Bengaluru
36. Commandant, ASTE (Aircraft & Systems Testing Establishment), Bengaluru
37. Army Avn Test Team (AATT), HAL, Marathahalli Post, Bangalore
38. The Chief of the Naval Staff
    [for **ACNSC(AM)]**
    IHQ MOD (Navy), 'A' Block
    Dalhousie Road South Avenue
    New Delhi.
39. The Commanding Officer, SDI, IAF, Kempapura, Yemalur Post, Bengaluru.
40. Regional Director, Office of RDAQA, C/o. ARDC, HAL, Bengaluru
41. GM (EW&A), BEL, Jalahalli Post, Bengaluru.
42. The Director, ALISDA, Jalahalli Camp Road, MES Road, Yeshwantapur, Bengaluru.
43. Director, NAL, Bengaluru
44. RD, RCMA (Hyd)
45. RD, RCMA (Materials)
46. RD, RCMA (Missiles)
47. RD, RCMA (Korwa)
48. RD, RCMA (Lucknow)
49. RD, RCMA (Nasik)
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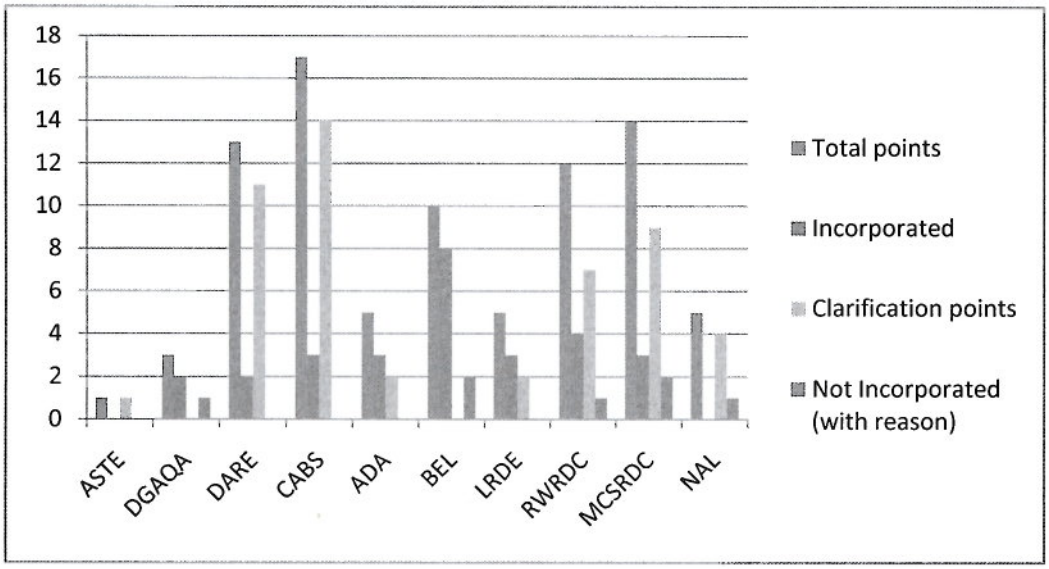
10. RD, RCMA (F&F-FOL)

FEEDBACK - CEH AW DIRECTIVE

(Feedback received from 10 organizations)

Sl No.	Date	Organization	Total points	Incorporated	Clarification points	Not Incorporated (with reason)
1	29-Jan-16	ASTE	**1**	0	1	0
2	25-Jan-16	DGAQA	**3**	2	0	1
3	18-Jan-16	DARE	**13**	2	11	0
4	14-Jan-16	CABS	**17**	3	14	0
5	30-Dec-15	ADA	**5**	3	2	0
6	30-Dec-15	BEL	**10**	8	0	2
7	21-Dec-15	LRDE	**5**	3	2	0
8	3-Mar-16	RWRDC	**12**	4	7	1
9	29-Feb-16	MCSRDC	**14**	3	9	2
10	29-Feb-16	NAL	**5**	0	4	1



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