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CEMILAC\_SYSGP\_SVP\_03

**Software Verification Plan  
of <LRU/System Name>  
for  
<Platform Name>**

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**Amendment History**

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## 1.0 Introduction

The Software Verification Plan (SVP) is a description of the verification procedures to be used to satisfy the software verification process objectives.

### 1.1 Purpose and Scope

The purpose of this document is to provide the activities to be carried out for verification and validation for the project <Project>. This document shall covers all requirements defined in Section 11.3 and Sec 6.0 of DO-178C

### 1.2 Applicable documents

Define the list of all applicable documents in following sections:

#### 1.2.1.1 External documents

Define the list of all applicable documents of external origin, relevant for this project.

#### 1.2.1.2 Internal documents

Define the list of all applicable documents of internal origin, relevant for this project

### 1.3 Part Number and Nomenclature

Define the details of all software components having unique part number and nomenclature to identify them through the software development life cycle.

### 1.4 Acronyms and Abbreviations

Define all the abbreviations and acronyms with their expanded names in this section.

## 2.0 System Overview

This section provides an overview of the system, including description of its functions along with block diagram.

## 3.0 Software Overview

This section provides an overview of the software, including description of its all major functions.

## 4.0 Organization:

Defined organizational responsibilities within the software verification process and interfaces with the other software life cycle processes.

## 5.0 Independence

A description of the methods for establishing verification independence, when required.

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## 6.0 Verification Methods

A description of the verification methods to be used for each activity of the software verification process.

### 6.1 Software Planning Process Verification methods

Description of documents/ data that are reviewed and analysed. Cover PSAC, SVP, SCMP, SDP, SQAP. Completeness of the plans and consistency among the plans. Include Input, Output, Transition Criteria, method and checklist(s) for the activity.

### 6.2 Software Requirement Process Verification methods

Description of documents/ data that are reviewed and analysed. Cover high level requirement correctness and completeness checks, traceability to system requirements, consistency within the requirements etc.

<Include Input, Output, Transition Criteria, method including checklist(s) and verification of evidence for achieving objectives under above verification process.>

### 6.3 Software Design Process Verification methods

Description of documents/ data that are reviewed and analysed. Cover software architecture, Low level requirement correctness and completeness checks, traceability to High level requirements, algorithm verification methods etc.

<Include Input, Output, Transition Criteria, method including checklist(s) and verification of evidence for achieving objectives under above verification process>

### 6.4 Software Coding Process Verification methods

Description of code that is reviewed and analysed. Cover code walkthrough, traceability to low level requirements, control & data flow checks for determinism, coding standard checks, robustness/ testability/ readability/ maintainability checks, no undocumented function implemented, stack usage, fixed point arithmetic overflow and resolution, resource contention, worst-case execution timing, exception handling, use of uninitialized variables or constants, unused variables or constants, and data corruption due to task or interrupt conflicts etc.

<Include Input, Output, Transition Criteria, method including checklist(s) and verification of evidence for achieving objectives under above verification process.>

### 6.5 Software Testing Process Verification methods

Description of test case preparation rationale, regression tests selection method, requirement based coverage, normal and abnormal conditions, external/ internal failure

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simulations, structural coverage, coverage analysis methods, test data to be produced for low level testing, integration testing, HSI testing, rig testing, aircraft testing etc.

<Include Input, Output, Transition Criteria, method including checklist(s) and verification of evidence for achieving objectives under above verification process

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## 7.0 Verification Environment

A description of the equipment for testing, the testing and analysis tools, and the guidelines for applying these tools and hardware test equipment, indicating target computer and simulator or emulator differences.

## 8.0 Transition Criteria

Define the transition criteria for entering the software verification process defined in this plan.

## 9.0 Partitioning Considerations

If partitioning is used, the methods used to verify the integrity of the partitioning.

## 10.0 Compiler Assumptions

A description of the assumptions made by the designer about the correctness of the compiler, linkage editor or loader.

## 11.0 Re-verification

For software modification, a description of the methods for identifying the affected areas of the software and the changed parts of the Executable Object Code. The re-verification should ensure that previously reported errors or classes of errors have been eliminated.

## 12.0 Previously Developed Software

For previously developed software, if the initial compliance baseline for the verification process does not comply with this document, a description of the methods to satisfy the objectives of this document.

## 13.0 Multiple-version Dissimilar Software

If multiple-version dissimilar software is used, define the description of the software verification process activities, as defined in Sec 12.3.2 of DO178 C.

## Appendix A Verification Checklist

<Define Verification Checklist for all SDLC phases that shall be used for verification activities and to generate SVP Records>.

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